

What is claimed is:

1. A method for forming a depletion mode p-channel memory cell, comprising:
forming an oxide layer having a thickness of less than 50 Angstroms (Å) on a substrate having a p-type doped channel region separating a source and a drain region in the substrate;
forming a floating gate on the oxide layer;
forming a dielectric layer on the floating gate; and
forming a control gate on the dielectric layer.
2. The method of claim 1, wherein forming the oxide layer includes forming the oxide layer to have a thickness of 23 Angstroms (Å).
3. The method of claim 1, wherein forming the floating gate includes forming a floating gate which has a bottom layer surface area of approximately 10^{-10} cm², and which is adapted to hold a fixed charge on the order of 10^{-17} Coulombs.
4. The method of claim 1, wherein forming the depletion mode p-channel memory cell includes forming a non volatile depletion mode p-channel memory cell, and wherein forming the floating gate includes forming a floating gate which is adapted to hold a fixed charge over a limited range of floating gate potentials.
5. The method of claim 1, wherein forming the floating gate includes forming an n+ type, heavily doped floating gate.
6. The method of claim 1, wherein forming the depletion mode p-channel memory cell includes forming the p-channel memory cell to operate at a voltage of approximately 1.0 Volts applied to the control gate.

7. A method for forming a depletion mode p-channel transistor, comprising:
forming an oxide layer having a thickness of less than 50 Angstroms (Å) on a substrate having a p-type doped channel region separating a source and a drain region in the substrate; and
forming a floating gate on the oxide layer, wherein the floating gate is adapted to hold a fixed charge over a limited range of floating gate potentials or electron energies.
8. The method of claim 7, wherein forming an oxide layer of less than 50 Angstroms (Å) includes forming the oxide layer to have a thickness of 23 Angstroms (Å).
9. The method of claim 7, wherein forming the floating gate further includes forming a floating gate which is adapted to hold a fixed charge on the order of 10^{-7} Coulombs over a range of floating gate potentials of +/- 1.0 Volts.
10. The method of claim 7, wherein forming the depletion mode p-channel transistor further includes forming an intergate dielectric on the floating gate and forming a control gate on the intergate dielectric.
11. The method of claim 7, wherein forming the depletion mode p-channel transistor includes forming the depletion mode p-channel transistor to have an operating voltage of less than 2.5 Volts across the oxide layer.
12. A method of forming a memory device, comprising:
forming a plurality of memory cells, wherein forming the plurality of memory cells includes forming at least one depletion mode p-channel memory cell, and wherein forming at least one depletion mode p-channel memory cell includes:
forming an oxide layer having a thickness of less than 50 Angstroms

(Å) on a substrate having a p-type doped channel region separating a source and a drain region in the substrate; and forming a floating gate on the oxide layer, and wherein forming the floating gate includes forming a floating gate which is adapted to hold a fixed charge over a range of floating gate potentials; and forming at least one sense amplifier, wherein forming at least one sense amplifier includes coupling the at least one amplifier to the plurality of memory cells.

13. The method of claim 12, wherein forming an oxide layer having a thickness of less than 50 Angstroms (Å) includes forming the oxide layer to have a thickness of 23 Angstroms (Å).

14. The method of claim 12, wherein forming the floating gate which is adapted to hold a fixed charge over a range of floating gate potentials includes forming a floating gate which is adapted to hold a fixed charge on the order of 10^{-17} Coulombs for a number of read operations on the order of 10^{15} cycles.

15. The method of claim 12, wherein forming the at least one depletion mode p-channel transistor further includes forming an intergate dielectric on the floating gate and forming a control gate on the intergate dielectric.

16. The method of claim 15, wherein forming the at least one depletion mode p-channel transistor further includes forming the depletion mode p-channel transistor to have an operating voltage of approximately 1.0 Volt.

17. The method of claim 12, wherein forming the floating gate which is adapted to hold a fixed charge over a range of floating gate potentials includes forming a

floating gate which is adapted to hold a fixed charge with an operating voltage of less than 2.5 Volts across the oxide layer.

18. A method for forming a non volatile depletion mode p-channel memory cell, comprising:

forming an oxide layer having a thickness of less than 50 Angstroms (Å) on a substrate having a p-type doped channel region separating a source and a drain region in the substrate;

forming an n+ type, heavily doped floating gate on the oxide layer;

forming a dielectric layer on the floating gate; and

forming a control gate on the dielectric layer,

wherein the memory cell is formed to hold a fixed charge on the floating gate over a limited range of floating gate potentials where electrons neither tunnel from nor tunnel to the floating gate.

19. The method of claim 18, wherein forming an oxide layer includes forming an oxide layer having a thickness of approximately 30 Angstroms (Å).

20. The method of claim 18, wherein forming an oxide layer includes forming an oxide layer having a thickness of approximately 23 Angstroms (Å).

21. The method of claim 18, wherein the fixed charge on the floating gate is on the order of 10^{-17} Coulombs.

22. A method for forming a non volatile depletion mode p-channel memory cell, comprising:

forming an oxide layer having a thickness of less than 50 Angstroms (Å) on a substrate having a p-type doped channel region separating a source and a drain region in the substrate;

forming an n+ type, heavily doped floating gate on the oxide layer where the floating gate has a bottom layer surface area of approximately 10^{-10} cm²;
forming a dielectric layer on the floating gate; and
forming a control gate on the dielectric layer,
wherein the memory cell is formed to hold a fixed charge on the order of 10^{-17} Coulombs on the floating gate over a limited range of floating gate potentials where electrons neither tunnel from nor tunnel to the floating gate, and is formed to operate at a voltage of approximately 1.0 Volts applied to the control gate.

23. The method of claim 22, wherein forming an oxide layer includes forming an oxide layer having a thickness of approximately 30 Angstroms (Å).

24. The method of claim 22, wherein forming an oxide layer includes forming an oxide layer having a thickness of approximately 23 Angstroms (Å).

25. A method for forming a depletion mode p-channel memory cell, comprising:
forming an oxide layer having a thickness of less than 50 Angstroms (Å) on a substrate having a p-type doped channel region separating a source and a drain region in the substrate;

forming a floating gate on the oxide layer;
forming a dielectric layer on the floating gate; and
forming a control gate on the dielectric layer,

wherein the memory cell is formed to have a limited range of floating gate potentials where electrons neither tunnel from nor tunnel to the floating gate, the limited range of floating gate potentials including:

a first potential reached when electrons tunnel to the floating gate
when a positive voltage is applied to the control gate, the first potential corresponding to a high conductivity state in the channel region; and

a second potential reached when electrons tunnel from the floating gate when a negative voltage is applied to the control gate, the second potential corresponding to a low conductivity state in the channel region.

26. The method of claim 25, wherein forming an oxide layer includes forming an oxide layer having a thickness of approximately 30 Angstroms (Å).

27. The method of claim 25, wherein forming an oxide layer includes forming an oxide layer having a thickness of approximately 23 Angstroms (Å).

28. The method of claim 25, wherein forming the floating gate includes forming a floating gate which has a bottom layer surface area of approximately 10^{-10} cm², the memory cell being formed to hold a fixed charge on the order of 10^{-17} Coulombs on the floating gate and to operate at a voltage of approximately 1.0 Volts applied to the control gate.

29. A method for forming a depletion mode p-channel memory cell, comprising:
forming an oxide layer having a thickness of less than 50 Angstroms (Å) on a substrate having a p-type doped channel region separating a source and a drain region in the substrate;

forming a floating gate on the oxide layer;

forming a dielectric layer on the floating gate; and

forming a control gate on the dielectric layer,

wherein the memory cell is formed to have a limited range of floating gate potentials where electrons neither tunnel from nor tunnel to the floating gate, the limited range of floating gate potentials including:

a first potential reached when electrons tunnel to the floating gate
when a positive voltage is applied to the control gate, the first

potential corresponding to a high conductivity state in the channel region; and

a second potential reached when electrons tunnel from the floating gate when a negative voltage is applied to the control gate, the second potential corresponding to a low conductivity state in the channel region,

wherein the memory cell is formed to hold a fixed charge on the floating gate over a range of floating gate potentials includes forming a floating gate which is adapted to hold a fixed charge on the order of 10^{-17} Coulombs for a number of read operations on the order of 10^{15} cycles, and to have an operating voltage of approximately 1.0 Volt.

30. The method of claim 29, wherein forming an oxide layer includes forming an oxide layer having a thickness of approximately 30 Angstroms (Å).

31. The method of claim 29, wherein forming an oxide layer includes forming an oxide layer having a thickness of approximately 23 Angstroms (Å).